REMARKS

The Applicant would like to thank the Examiner for the thorough examination of the present application, and for correctly indicating as allowable the subject matter of dependent Claims 17, 21, 28 and 34.

Independent Claims 13 and 19 have been amended to recite that the verification circuit cooperates with the precharging register. In addition, Claim 16 has been amended to change its dependency as helpfully noted by the Examiner. These amendments do not narrow the scope of the claims for any reasons relating to patentability.

The arguments supporting patentability of the claims are presented below.

I. The Claimed Invention

The present invention as recited in independent Claim 13, for example, is directed to a decoding circuit for decoding a biphase signal having a pair of states. The decoding circuit comprises a precharging register for precharging respective states of the biphase signal, with one state of the pair of states being precharged at each pulse of a periodic precharging signal. A verification circuit cooperates with the precharging register for comparing the two states of the pair of states to detect an error. The verification circuit also provides an error signal when the two states are equal indicating that they have

not been received accurately.

Independent Claims 19 and 23 are directed to related circuits, and independent Claim 30 is directed to a related method.

II. The Claims Are Patentable

The Examiner rejected independent Claims 13, 19, 23 and 30 over the Hiramatsu patent. The Hiramatsu patent discloses a circuit for decoding bi-phase BPSK signals. The Applicant submits that the Examiner has mischaracterized the Hiramatsu patent.

First, the Examiner characterized the shift register **31** as a precharging register for precharging respective states of the biphase signal, with one state of the pair of states being precharged at each pulse of a periodic precharging signal - as in the clamed invention. The Applicant submits that the Hiramatsu patent fails to teach or suggest that the respective states of the biphase signal are precharged. Reference is directed to column 1, line 62 to column 2, lines 7 of the Hiramatsu patent which provides:

> "Shift register **31** applies continuous three half bits of the successively input bi-phase signal **a** to EXNOR gate **32** and EXOR gate **33**, in which every two bits are compared with each other. An output from EXOR gate **32** is applied to one input end of an AND gate **34** and to one input end of an NOR gate **35**, while an output from EXOR gate **33** is applied to the

> other input end of AND gate **34** and to the other input end of NOR gate **35**. Of the half bits **a0**, **a1** and **a2** in shift register **31**, when **a0** and **a1** are the same, the output from EXOR gate **32** attains to "1", and when half bits **a1** and **a2** are different from each other, the output from EXOR gate **33** also attains to "1", and hence the output from AND gate **34** attains to "1". (Emphasis added).

As noted above, the shift register **31** simply operates as a shift register without performing any precharging of the half buts **a0**, **a1** and **a2**. In sharp contrast, independent Claim 13 recites a precharging register for "precharging respective states of the biphase signal, with one state of the pair of states being precharged at each pulse of a periodic precharging signal."

Secondly, independent Claim 13 recites that the verification circuit cooperates with the precharging register for comparing the two states of the pair of states to detect an error, and providing an error signal when the two states are equal indicating that they have not been received accurately.

The error detected in Hiramatsu determines when 3 bits of data received by the shift register **31** cannot be paired. This is different than determining if the two states of the biphase signal have not been received accurately. In Hiramatsu, to determine if the 3 bits of data cannot be paired, two comparisons are necessary to detect an eventual error, namely ai with ai+1 and ai+1 with ai+2. An error signal is provided only if it is not possible to determine which states should be paired, i.e., if ai

does not equal ai+1 and ai+1 does not equal ai+2. Reference is directed to column 6, lines 41-48 of Hiramatsu, which provides:

> "Further, if 3 bits of data assumes "010" and the outputs from logic operation circuit **40** are X=0 and Y=0 by some cause, updown counter **41** neither counts up nor counts down. However, as long as the count value is larger than the prescribed threshold value α1=1 of the first comparator **42**, the circuit determines that there is error in the three bits of data, and continues to determine the pairs as (**a0**, **a1**), (**a2**, **a3**), (**a4**, **a5**) … , similar to the aforementioned example." (Emphasis added).

Thus, in the circuit of Hiramatsu, two comparisons are necessary to detect an eventual error, and an error is detected if ai does not equal ai+1 and ai+1 does not equal ai+2. In sharp contrast, an error signal is provided when the two states are equal indicating that they have not been received accurately.

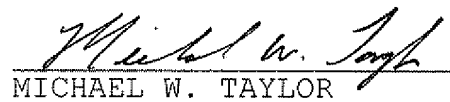
Accordingly, it is submitted that independent Claim 13 is patentable over the Hiramatsu patent. Independent Claims 19, 23 and 30 are similar to amended independent Claim 13. Therefore, it is submitted that these claims are also patentable over the Hiramatsu patent.

In view of the patentability of independent Claims 13, 19, 23 and 30, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

III. Conclusion

In view of the amendments to the claims and the arguments presented above, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,



MICHAEL W. TAYLOR
Reg. No. 43,182
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330